REMARKS/ARGUMENTS

Claims 1-11 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Shiozawa in view of Yamaguchi.

Claim 1 comprises the limitations of:

forming a trench isolation structure and an active region proximate an outer surface of a semiconductor layer;

depositing an epitaxial layer outwardly from the trench isolation structure;

growing a first insulator layer outwardly from the epitaxial layer;

growing a second insulator layer outwardly from the first insulator layer;

forming a gate stack outwardly from the epitaxial layer, the gate stack comprising a portion of the first insulator layer, a portion of the second insulator layer, and a gate formed proximate the second insulator layer, the gate having a narrow region and a wide region; and

heating the epitaxial layer to a temperature sufficient to allow for the epitaxial layer to form a source/drain implant region in the active region.

In forming the rejection to claim 1 the examiner states, " (Shiozawa fig. 3b # 141, col. Col.5 line 11) growing a first insulator layer outwardly from the epitaxial layer; (Shiozawa fig. 3b # 127) growing a second insulator layer outwardly from the first insulator layer; ". The examiner has interpreted layer 141 in Fig 3(b) of the Shiozawa patent to represent the first insulator layer. The examiner then interprets layer 127 in Fig. 3(b) to represent the growing of the second insulator layer outwardly from the first insulator layer. The examiner is directed to Fig. 3(b) which shows the position of layer 127 to be between the substrate 113 and the gate layer 125a. Figure 3(b) also shows that the layer 141, which the examiner interprets to be the first insulator layer, is actually formed adjacent to and above layer 127. The Shiozawa patent therefore does not describe forming layer 127 outward from layer 141 as described by the examiner. The Yamamguchi patent, with which the examiner combines the Shiozawa patent, also does not teach the required limitations of claim 1. In particular, the Yamamguchi patent does

not show that a second insulator layer is grown outwardly from the first insulator layer. All the required elements of the claimed invention are not found in the combined references and claim 1 is allowable over the cited art under 35 U.S.C. 103. Furthermore, claims 2-11 depend from claim 1 and therefore contain all the limitations of claim 1. Claims 2-11 are therefore also allowable over the cited art.

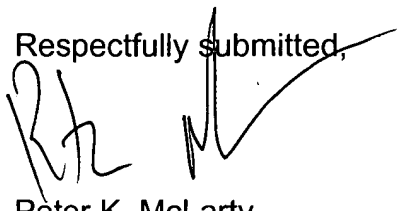
Applicants appreciate the indication that claims 12 and 13 are allowed.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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Amendments to the Drawings:

None